

Figure 1

Integrated system

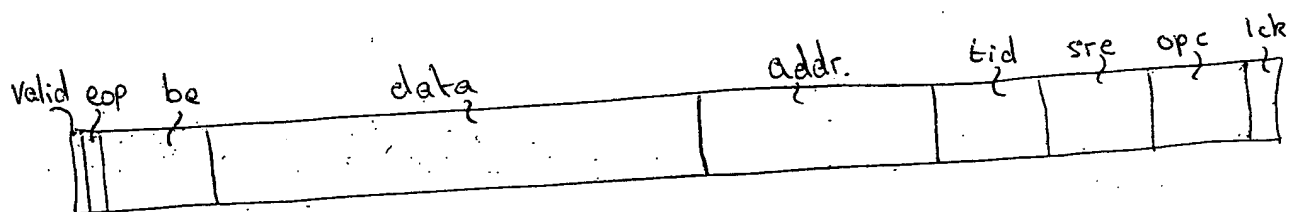
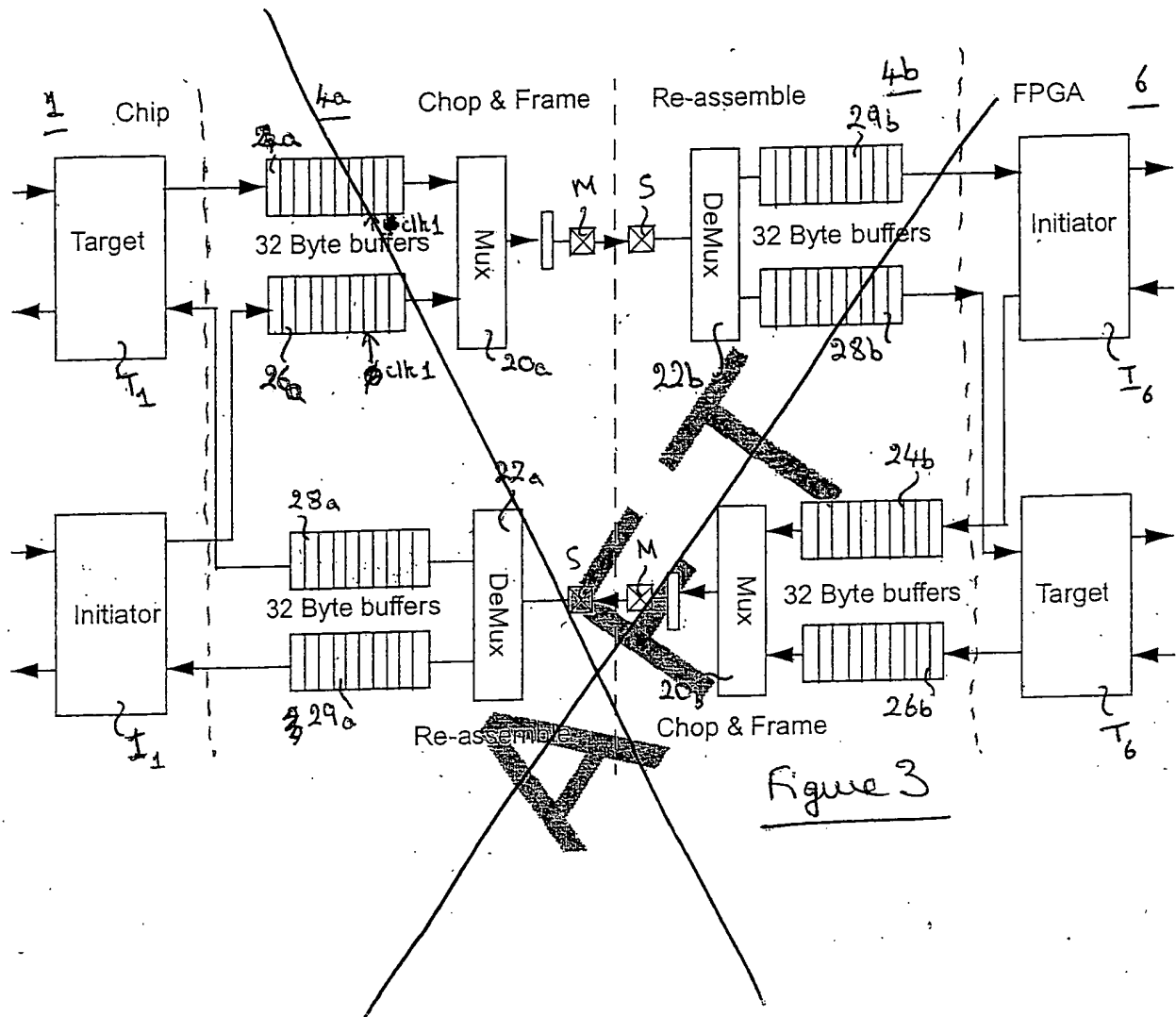


Figure 2

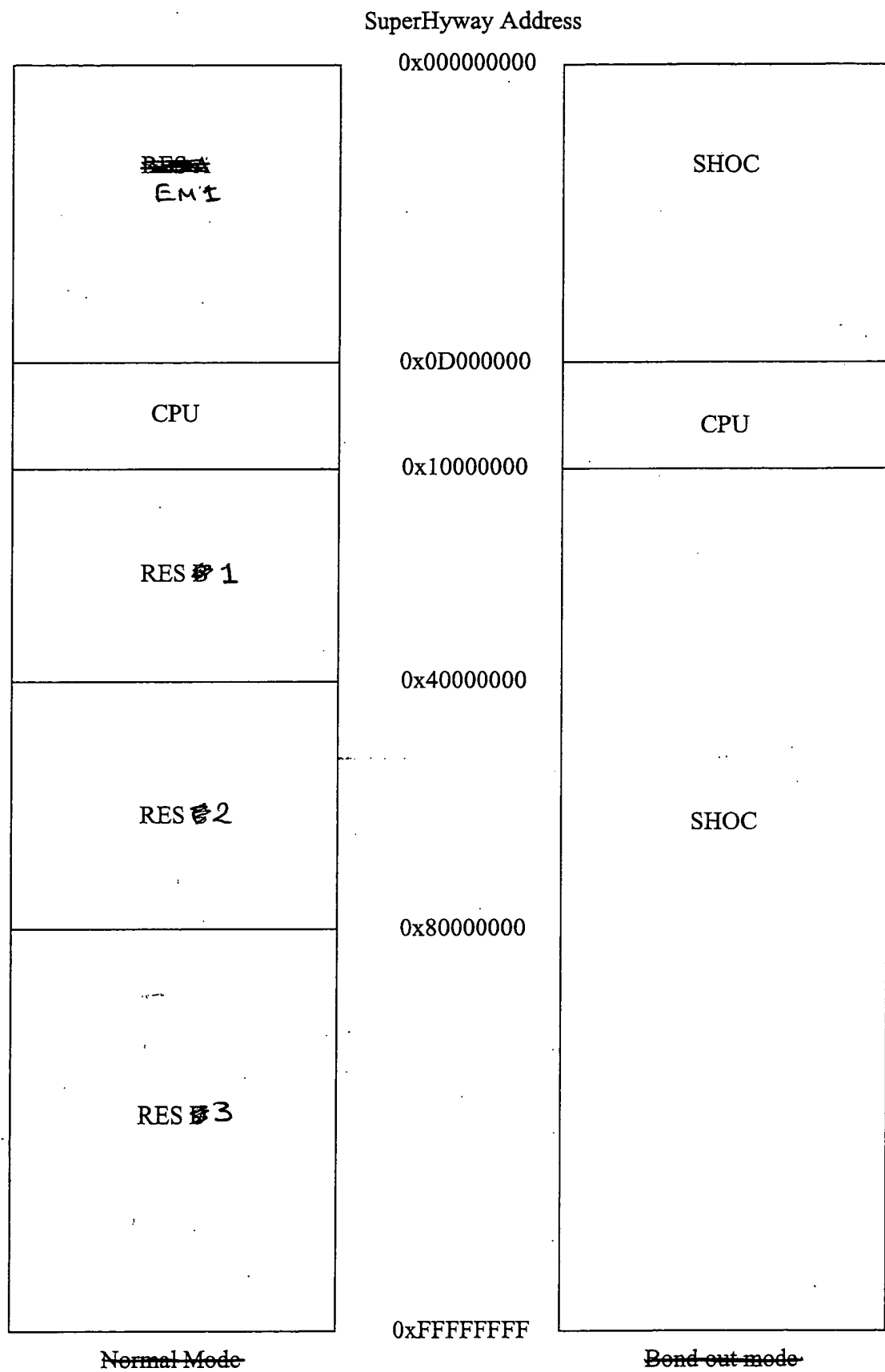


Figure 3

Dual Address maps

Figure 4

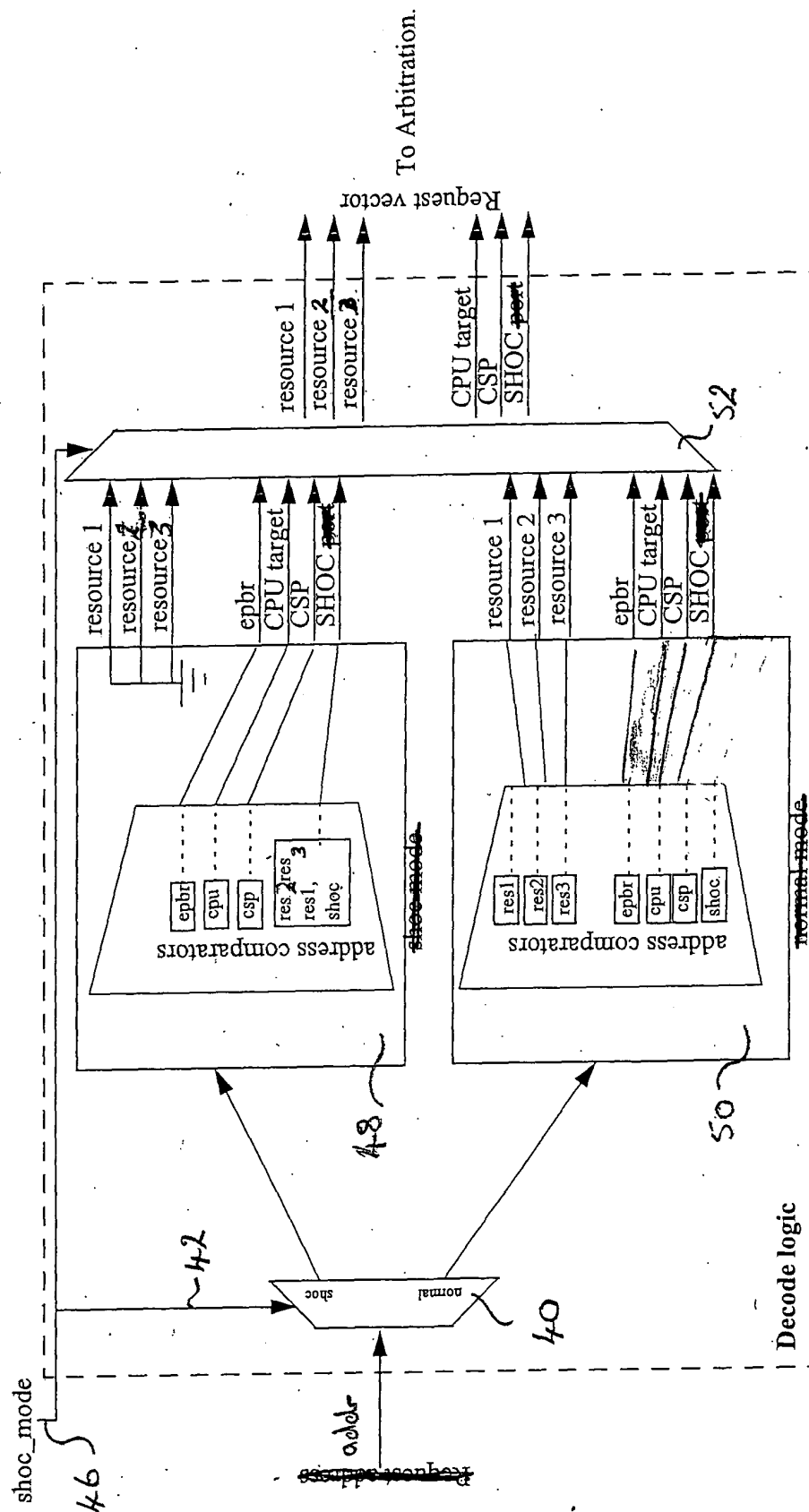


Figure 5